WHAT IS CLAIMED IS:

1. A memory, comprising:

an array of memory cells; and

a control circuit configured to read error correction coded data from the array of memory cells, provide error correction code decoding to selected error correction coded data and discard unused error correction code parity data of unselected error correction coded data.

2. The memory of claim 1, where the control circuit is configured to check the integrity of the error correction coded data and provide error correction code decoding to error correction coded data that has compromised integrity.

3. The memory of claim 1, where the control circuit is configured to calculate a checksum of the error correction coded data, compare the calculated checksum to a retrieved checksum and provide error correction code decoding to error correction coded data if the calculated checksum differs from the retrieved checksum.

4. The memory of claim 1, where the control circuit is configured to calculate odd/even parity of the error correction coded data, compare the calculated odd/even parity to an expected odd/even parity and provide error correction code decoding to error correction coded data if the calculated odd/even parity differs from the expected odd/even parity.

5. The memory of claim 1, where the control circuit is configured to evaluate parametric data from the array of memory cells and provide error correction code decoding to error correction coded data based on the parametric data evaluation.

6. The memory of claim 1, where the control circuit comprises a memory buffer configured to receive the error correction coded data, provide the selected

error correction coded data to an error correction code decoder and provide the unselected error correction coded data to a buffer circuit configured to discard the unused error correction parity data of the unselected error correction coded data.

7. The memory of claim 1, where the control circuit is configured to provide a Reed-Solomon error correction code.

8. The memory of claim 1, where the array of memory cells is a macro-array of magnetic memory cells.

9. The memory of claim 1, where the array of memory cells is a phase-change random access memory array of memory cells.

10. The memory of claim 1, where the array of memory cells is a FLASH random access memory array of memory cells.

11. The memory of claim 1, where the array of memory cells is a probe based memory array of memory cells.

12. A magnetic memory, comprising:

a macro-array of memory cells; and

a control circuit configured to read the macro-array of memory cells to obtain ECC encoded data comprising ECC parity data, evaluate the ECC encoded data reliability while leaving the ECC parity data idle, and provide error correction decoding to the ECC encoded data based on the reliability evaluation.

13. The magnetic memory of claim 12, where the control circuit is configured to evaluate the ECC encoded data reliability using resistance readings from the macro-array of memory cells.

14. The magnetic memory of claim 12, where the control circuit is configured to evaluate the ECC encoded data reliability using resistance readings from test memory cells in the macro-array of memory cells.

15. The magnetic memory of claim 12, where the control circuit is configured to evaluate the ECC encoded data reliability using logic states from memory cells in the macro-array of memory cells.

16. The magnetic memory of claim 12, where the control circuit is configured to evaluate the ECC encoded data reliability using a CRC checksum of the ECC encoded data.

17. The magnetic memory of claim 12, where the control circuit is configured to store a CRC checksum next to each codeword of the ECC encoded data.

18. The magnetic memory of claim 12, where the control circuit is configured to store a group of original data next to a group of ECC parity data that is next to a group of CRC checksums.

19. The magnetic memory of claim 12, where the control circuit comprises:

a processor;

a storage interface configured to communicate with the macro-array of memory cells; and

a buffer circuit comprising a buffer memory.

20. The magnetic memory of claim 19, where the storage interface is configured to evaluate the ECC encoded data reliability and select the ECC encoded data for error correction decoding, where the processor is configured to evaluate the ECC encoded data reliability and select the ECC encoded data for error correction decoding, where the buffer circuit is configured to discard idle ECC parity data, where the storage interface is configured to provide CRC

encoding, CRC decoding and discarding of CRC checksums, and where the storage interface is configured to provide error correction encoding of original data.

21. A magnetic memory, comprising:
means for storing data encoded with an ECC scheme;
means for reading the ECC encoded data;
means for identifying corrupted ECC encoded data; and
means for decoding the identified corrupted ECC encoded data.

22. The magnetic memory of claim 21, where the means for identifying corrupted ECC encoded data comprises evaluating at least one from a group comprising:
logic states of memory cells;
parametric values of memory cells;
an odd/even parity check of the ECC encoded data; and
a checksum of the ECC encoded data.

23. The magnetic memory of claim 21, where the means for decoding comprises:
a buffer circuit configured to provide corrupted ECC encoded data to an ECC decoding unit and discard ECC parity data of uncorrupted ECC encoded data.

24. The magnetic memory of claim 21, where the means for decoding comprises a Reed-Solomon ECC decoding unit.

25. The magnetic memory of claim 21, where the means for decoding comprises a BCH ECC decoding unit.

26. A method for writing to and reading from a magnetic memory, comprising:
reading ECC encoded data from the memory;

evaluating non-ECC parity data to obtain an evaluation result; and

decoding the ECC encoded data to obtain recovered data if the evaluation result indicates the ECC encoded data is corrupted.

27. The method of claim 26, comprising:

receiving original data;

encoding the received original data with an ECC scheme;

calculating CRC checksums for the ECC encoded data; and

writing the ECC encoded data and the CRC checksums into the memory.

28. The method of claim 27, where reading ECC encoded data comprises retrieving the ECC encoded data and the CRC checksums, and evaluating non-ECC parity data comprises:

calculating CRC checksums for the ECC encoded data; and

comparing the calculated CRC checksums to the retrieved CRC checksums to obtain compare results that indicate whether the ECC encoded data is corrupted.

29. The method of claim 26, comprising:

providing recovered data from corrupted ECC encoded data;

discarding the ECC parity data from uncorrupted ECC encoded data; and

providing original data from the uncorrupted ECC encoded data.